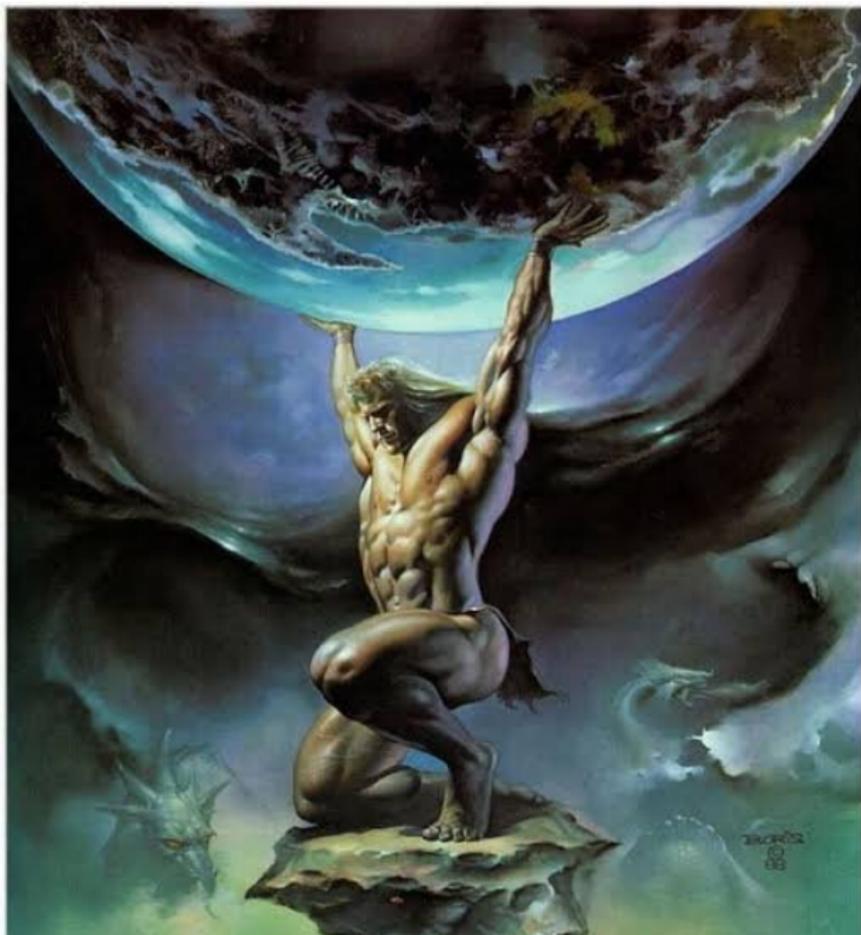


wat: hardware edition

Emil J / widlarizer

TCL



TCL

```
1  emil@blahaj ~> tclsh
2  % set x 1
3  1
4  % set x $x+1
```

TCL

```
1  emil@blahaj ~> tclsh
2  % set x 1
3  1
4  % set x $x+1
5  1+1
```

TCL

```
1  emil@blahaj ~> tclsh
2  % set x 1
3  1
4  % incr x
5  2
```

TCL

... there is no syntax, or it's so simple you have to do everything outside the syntax.

- Guido van Rossum, 1999

It was designed to be a “scripting language”, on the assumption that a “scripting language” need not try to be a real programming language. ... It lacks arrays; ... It fakes having numbers, which works, but has to be slow.

- GNU Jesus, 1994

There are people at the office who have been dealing with this crap for 20 years and still can't tell me off the top of their head the order of parameters to basic functionality functions.

- some guy on orange site

Verilog

Verilog

1 and _2_ compute different values. Credit: @whitequark

```
1 module top(a, b, c);
2     input a;
3     input [2:0] b;
4     input [3:0] c;
5     wire [3:0] _0_;
6     wire [3:0] _1_;
7     wire [3:0] _2_;
8     assign _0_ = + $signed(b);
9     assign _1_ = a ? _0_ : c;
10    assign _2_ = a ? (+ $signed(b)) : c;
11 endmodule
```

Verilog

+m Unary plus m (same as m)

- ▶ IEEE 1364 Verilog HDL

For the arithmetic operators, if any operand bit value is the unknown value **x** or the high-impedance value **z**, then the entire result value shall be **x**.

- ▶ also IEEE 1364 Verilog HDL

Table 17-5—Mnemonics for strength levels

Mnemonic	Strength name	Strength level
Su	Supply drive	7
St	Strong drive	6
Pu	Pull drive	5
La	Large capacitor	4
We	Weak drive	3
Me	Medium capacitor	2
Sm	Small capacitor	1

Verilog

wire vs reg

???

Verilog

- ▶ one (1) good parser
- ▶ others so bad they literally crash your GUI
- ▶ “safe subset”
- ▶ IR?!
- ▶ every sufficiently complex HW design contains a verilog codegen
- ▶ non-synthesizable Verilog

Xilinx Vivado 2020.3
Total Size of download: 49.76 GB

3 Text files of the exact same EULA. 1.3GB each.

only supports 2 devices

Have to download 2020.2 with "updates" = 70.2 GB

Vivado Design Suite - HLS Edition - 2020.3 Full Product Installation

Important Information
 Download Vivado Design Suite 2020.3 now with support for:

- Production Devices
 - Xilinx® Kintex UltraScale™ (Kintex UltraScale™, Kintex UltraScale™ Pro)
 - Xilinx® Virtex UltraScale™ (Virtex UltraScale™, Virtex UltraScale™ Pro)

We strongly recommend to use the web-installer as it reduces download time and saves significant disk space.

Please see [hardware information](#) for details.

IMPORTANT NOTE: This release supports **2 dual device only!**
 For customers using dual devices, 3GB is recommended including Vivado 2020.3. For single devices, please continue to use Vivado 2020.2.

Note: Download web-installer is only supported with Google Chrome and Microsoft Edge web browsers.

Figure 3: Xilinx Vivado, 3k USD



Dadibom 09/12/2021

wtf why doesnt undo work in modelsim

i press ctrl+z to undo something and it deletes the entire contents of the file
and i cant redo

Figure 4: Modelsim

- ▶ nevermind, TCL is fine actually

Fine Dining



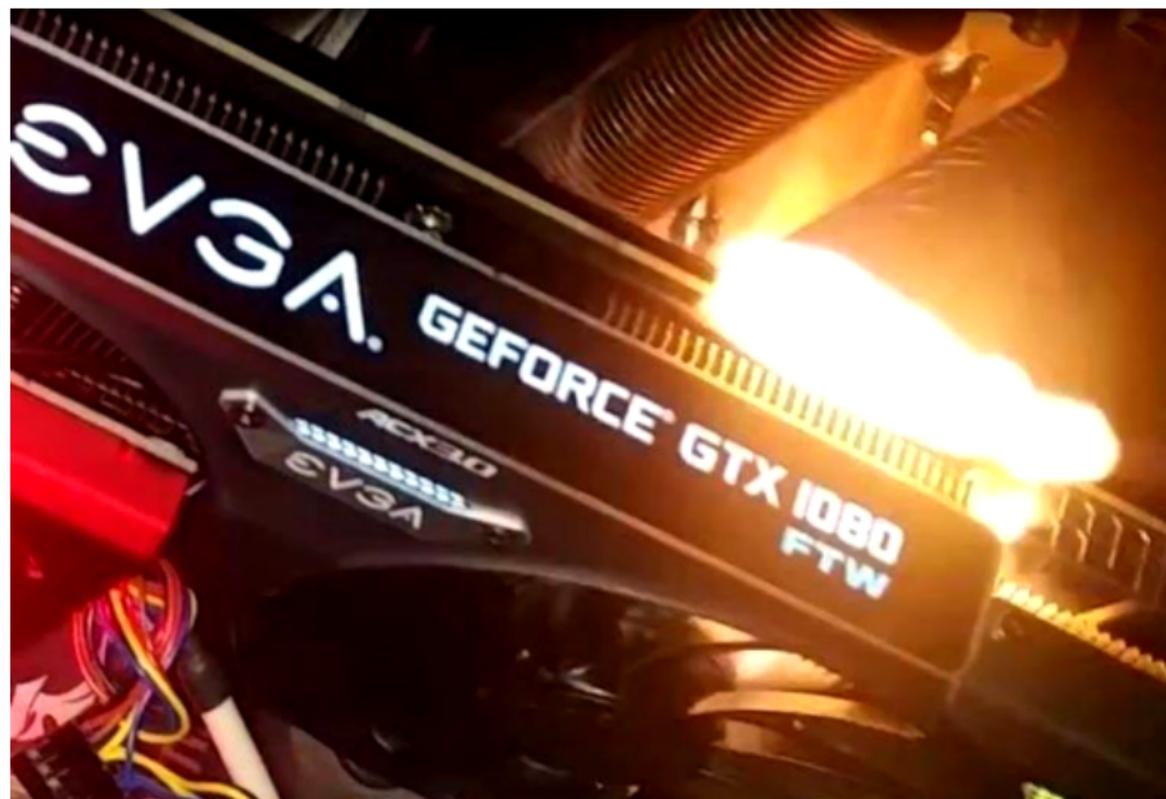
Figure 5: warnings

```
3221 set_property src_info {type:SCOPED_XDC file:87 line:13 export:INPL
3222 # Xilinx, and to the maximum extent permitted by applicable
3223 set_property src_info {type:SCOPED_XDC file:87 line:14 export:INPL
3224 # law: (1) THESE MATERIALS ARE MADE AVAILABLE "AS IS" AND
3225 set_property src_info {type:SCOPED_XDC file:87 line:15 export:INPL
3226 # WITH ALL FAULTS, AND XILINX HEREBY DISCLAIMS ALL WARRANTIES
3227 set_property src_info {type:SCOPED_XDC file:87 line:16 export:INPL
3228 # AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING
3229 set_property src_info {type:SCOPED_XDC file:87 line:17 export:INPL
3230 # BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-
3231 set_property src_info {type:SCOPED_XDC file:87 line:18 export:INPL
3232 # INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and
3233 set_property src_info {type:SCOPED_XDC file:87 line:19 export:INPL
3234 # (2) Xilinx shall not be liable (whether in contract or tort,
3235 set_property src_info {type:SCOPED_XDC file:87 line:20 export:INPL
3236 # including negligence, or under any other theory of
3237 set_property src_info {type:SCOPED_XDC file:87 line:21 export:INPL
3238 # liability) for any loss or damage of any kind or nature
3239 set_property src_info {type:SCOPED_XDC file:87 line:22 export:INPL
3240 # related to, arising under or in connection with these
3241 set_property src_info {type:SCOPED_XDC file:87 line:23 export:INPL
```

Figure 6: codegen wat

Hardware

You want to see side effects? I'll show you side effects



Hardware

AWS PUBLIC SECTOR SUMMIT

FPGA Acceleration Using F1

The diagram illustrates the workflow for FPGA acceleration on an EC2 F1 instance. It starts with an Amazon Machine Image (AMI) and an Amazon FPGA Image (AFI). These are used to launch an EC2 F1 instance and load the AFI. The instance then runs a CPU application on the F1, which is connected to the FPGA via a PCIe link. The FPGA is also connected to DDR controllers and DDR-4 attached memory via an FPGA link.

Amazon Machine Image (AMI)

EC2 F1 Instance

Launch Instance and Load AFI

Amazon FPGA Image (AFI)

CPU Application on F1

PCIe

UltraScale

DDR Controllers

FPGA Link

DDR-4 Attached Memory

Different AFIs can be loaded and reloaded on an F1 instance

An AFI can be loaded into the FPGA in less than 1 second

amazon web services

Figure 8: AWS F1

Hardware

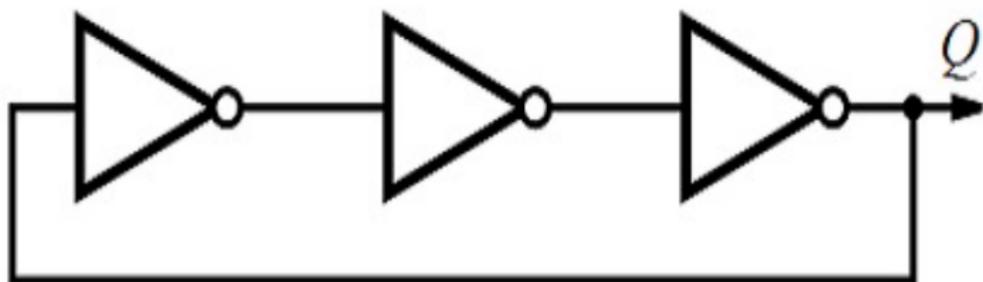
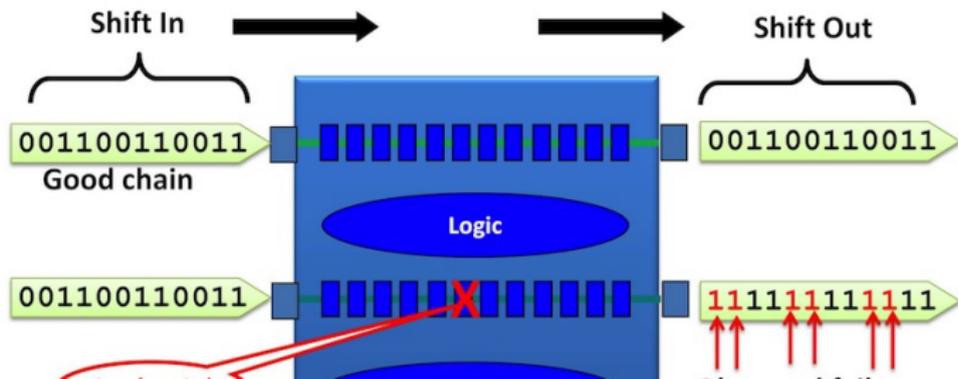


Figure 9: Ring oscillator

Hardware

When the response to a test vector is captured by state elements in scan based tests, the switching activity of the circuit may be large resulting in abnormal power dissipation and supply current demand.

- 10.1109/TEST.2006.297694



Hardware bugs

Always read the errata.

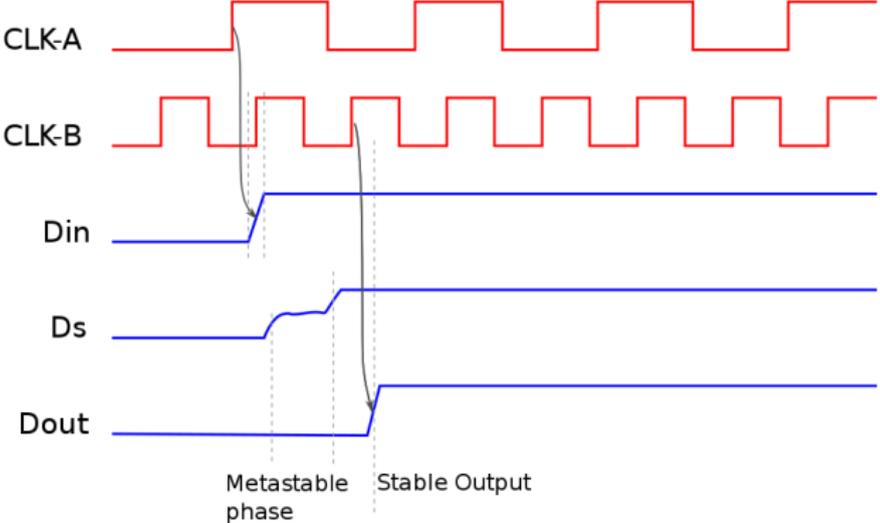
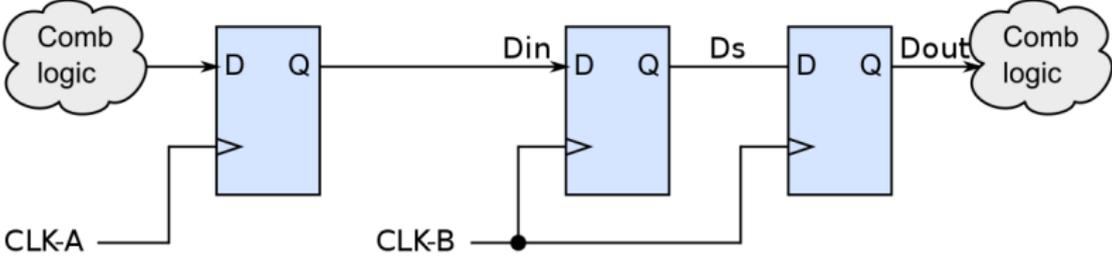
I2C: In master receive mode, data remains latched in data register until new data is received.

Workaround: When slave is configured to transmit data on an irregular basis, it should not send 2 consecutive bytes with the same data

- ▶ STM SPC582Bz automotive qualified certified microcontroller errata

...how do I submit a pull request against a piece of melted sand?

Hardware bugs



What now?

- ▶ better languages! Clash, Chisel, Amaranth
- ▶ tooling? Yosys, simulators, place-and-route, ASIC fab stuff, formal verification
- ▶ industry-standard isn't all there is
- ▶ hardware *can* be fun
- ▶ small world with tough problems